4. RAMCHECK OPERATION

This section outlines the operation of RAMCHECK. It instructs you on how to handle the socket, and describes the RAMCHECK tests in some detail. We strongly recommend that you read at least this section before putting the manual away. Please note that actual screen displays may vary as RAMCHECK's firmware is modified, or if you swap adapters.

4.1 INSERTION AND REMOVAL OF MODULES

1. Do not insert or remove a module when the Module Power red LED is on! (Press ESC to turn it off prior to insertion/removal.)

2. Never use excessive force to insert a DIMM module. If a module is not sliding in smoothly - please review the instructions on this page.

INSERTION:

Make sure the Module Power **red** LED is off (if not - press ESC). RAMCHECK uses a vertically mounted high-quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DIMM into the socket, pushing it evenly along its top. When the DIMM is properly inserted, the ejectors will snap onto the semi-circular notches on each side of the module.

REMOVAL:

Make sure that the Module Power **red** LED is off (if not - press ESC). In certain modules, the **red** LED may still be glowing slightly, even when the tester is in Standby Mode; if this occurs, it is still safe to remove the module from the socket (only in Standby Mode), as the module is allowing only a minor amount of leakage current to flow. This however, should not be interpreted as an indication of a defective device.

Place one finger on top of the DIMM module to **prevent the module from popping upward** and simultaneously pull both ejectors sideways.

NOTE: The socket used is of the best available quality. It is rated for 10,000 to 30,000 cycles of removal and insertion. Using it carefully will provide you with a long period of use. In particular, do not subject it to humidity and always follow the above instructions for smooth handling.

Replacement test socket are available for purchase.

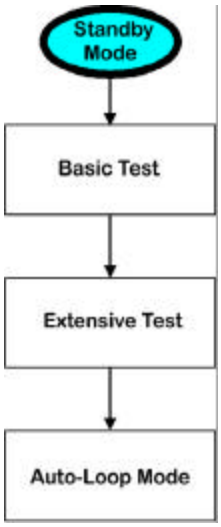
4.2 TEST PHASES

The main tests of RAMCHECK, the BASIC test, the EXTENSIVE test, and the AUTO-LOOP are MULTI-BYTE tests where all the data bus bits are checked simultaneously.

RAMCHECK starts with the BASIC test, which lasts between 3 and 60 seconds, depending on module size and type. The EXTENSIVE test automatically follows the BASIC test and it lasts several minutes. It includes different voltage and temperature related test procedures, as well as mode analysis. The AUTO-LOOP test proceeds in an endless loop of varying pattern (and algorithm) tests.

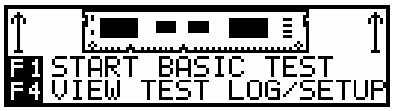
The following sub-sections describe each of the default main test phases: BASIC, EXTENSIVE, AUTO-LOOP.

Section 5 describes the RAMCHECK SETUP mode, which allows you to perform advanced tests in which you setup your own parameters and testflow.



4.2.1 STANDBY MODE

RAMCHECK's starting screen begins in the STANDBY mode where you are prompted with the following message to insert a module and start the test:

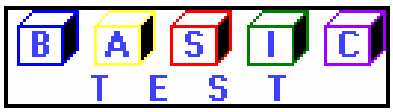


During this mode, no devices are being tested, and RAMCHECK internally tries to reduce its own power consumption.

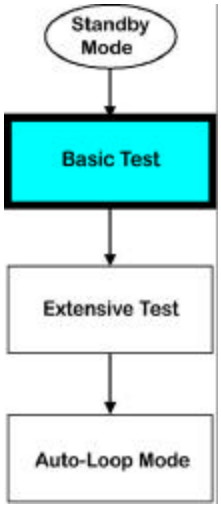
From STANDBY mode, you may select the following actions:

F1 - starts the automatic test as described in the following sections.
F2 - allows you access to all of RAMCHECK's advanced setup functions, which are described in Section 5.
F3 - run the DEMO program.
F4 -allows you to view the Test Log, to view any modified setup of RAMCHECK, or to access the SPD management program.
The **Test Log** is a unique feature of RAMCHECK. It is actually a scrollable list of all the results obtained during the last test. The information in the Test Log is retained until you perform a new test.
F5 -is used by our technical personnel to run RAMCHECK's extensive diagnostic programs.

4.2.2 BASIC TEST



The initial group of tests recognizes the memory type (DDR2, DDR, SDRAM, etc.) and determines the module size and DDR/SDRAM



frequency rate (or speed/cycle time for EDO/FPM). This group looks for basic wiring, addressing, and defective bit problems. If a problem is detected, the test is halted with the corresponding error message. If no initial problem is detected, the test continues with every cell being written to and read from with different basic bit patterns.

During the BASIC test, the graphic display shows animation depicting the progress of the test, a test timer, module type, size and speed. Speed is shown as the frequency in MHz for DDR2, DDR1 and SDRAM devices.

DDR2

DDR1

SDRAM

Please review our on-line manual addendum for a detailed description of the new DDR2 as well as the DDR1 Basic Test operation.

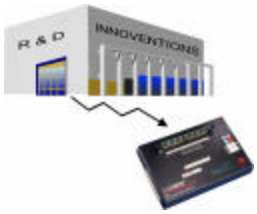
Legacy EDO/FPM devices show speed as access time and cycle time in nanosecond (nS). For example, the shortened notation 44/100nS on the following left screen indicates access time of 44nS with a cycle time of 100nS.

You will also note the '3_V' voltage indicator next to the access and cycle time. The '3_V' (or the '5_V' in the right screen) marks indicate that the device under test (DUT) is being tested at 3.3V (or 5V). SDRAM devices are exclusively tested at 3.3V, as shown in the following screen. The DDR2 and DDR1 adapters provide similar '$2^5{}_V$' and '$1^8{}_V$' markers together with more explicit voltage information (e.g. 2.90V). s

The animation characters show the DUT at bit or bytes resolution. In the left example we have tested an x64 device, which requires eight animation characters representing eight bytes of memory. The x72 module captured on the right screen requires nine. Similarly, an x40 module will require 5 byte-animation characters. The Basic Test in progress screen also displays the HEX code of the current test pattern used on the top right corner.

RAMCHECK performs numerous timing tests at the start of the BASIC test in order to determine the frequency of the DDR or SDRAM modules. Once the frequency is determined, RAMCHECK will commence to test the entire memory module at the selected

The frequency list is dependent on the DUT and is subject to change with firmware development.



frequency. If a problem is encountered, RAMCHECK will automatically reduce the frequency (e.g. 667MHz, 600MHz, 533MHz, 466MHz, and 400MHz for DDR2 devices), unless you have set up RAMCHECK to test at a fixed frequency by either Setup or the Change-on-the-fly feature.

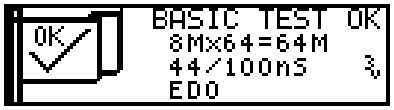
During the BASIC test, the screen will inform you of the voltage used to test the module, and display a constant change of patterns used to test it. When a group of patterns are used, only the first pattern is shown. The display shows an indication of "UBF" if the module is detected as unbuffered, while registered modules are identified with "REG". There are two LEDs next to the display on RAMCHECK. You will note that the MODULE POWER LED indicator will glow when a module is being tested, additionally, when testing DDR2 or SDRAM devices, you may see the Page Burst LED flash as memory patterns are bursted into the device at real clock rates.

Some devices utilize different wiring or addressing variations of the original JEDEC standard. This variation is legitimate on specific motherboards, but may result in failure in other motherboards that do not support this variation. If RAMCHECK encounters such a legitimate variation, it will flash a short warning message as in the following screen:

But it will not stop the test, as this module will work perfectly in all motherboards that support the 4K-refresh feature.

Successful Basic Test:

If the module passes the BASIC test, a few summary screens will follow to provide additional information on the module tested, including a translation of the JEDEC notation to the module size in whole.



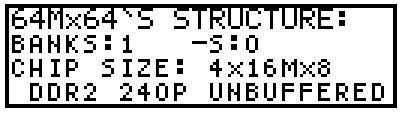
Detailed Structure Information:

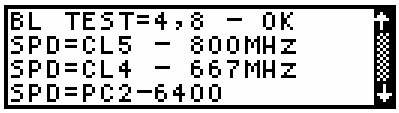
After passing the BASIC test, RAMCHECK displays a BASIC TEST OK message which is followed by a series of summary screens detailing speed and structure information.

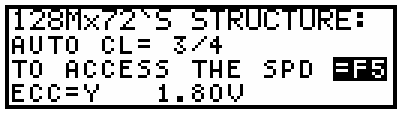
Please note that if you want to reach the summary screens quickly, even before the end of the Basic Test, simply abort the test by pressing F5 during the Basic Test.

You can also activate these structure screens by pressing F5 during the BASIC test.

The following screens show typical test results for modern DDR2 devices. Detailed manual addendums for both DDR2 and DDR1 basic test are continually updated on our web site www.innoventions.com. Users of the DDR2/1 adapters are encouraged to read those current manuals.

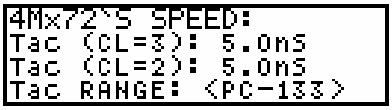


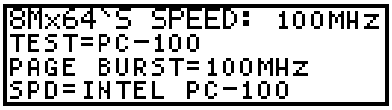


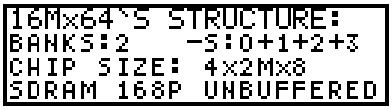


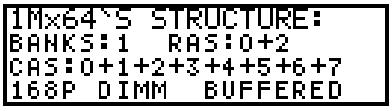
Please note that the fourth screen allows you to access the SPD using F5. Advanced users can use the powerful SPD management as detailed in our on-line manual.

The following screens demonstrate SDRAM test results. The first screen shows the measurements of Tac (access time from clock) for CAS latency 2 and 3. In the second screen, RAMCHECK determines speed compliance as the header "TEST=" is followed by "PC-100" or "PC-133". The third screen shows the size of the module, its type, number of the module's banks (or ranks), the use of the -S control lines, and the size of the individual chips used in the module. The module is an unbuffered 16Mx64 SDRAM with two banks, using control lines S0, S1, S2, and S3, and employing 4x2Mx8 chips.









Finally, we demonstrate the legacy EDO/FPM test results with a 168-pin buffered module using one bank and two RAS control lines.

All the test results are stored in the Test Log. You can view the Test Log of the previous test by pressing F4, F1 from Standby.

The Test Log

Please keep in mind that all speed and structure information is automatically recorded into the Test Log, which is accessible by pressing F4 from standby after the test. The information is retained in the Test Log until a new test is initiated. The results from Extensive and Auto-Loop are also recorded.

The Test Log is conveniently copied to the PC when you use the PC Real Time interface described in Section 6.

Samples of the test summary and the Test Log data for DDR1 modules are shown in the following screens:

```
128Mx64`S STRUCTURE:
DEFAULT:CL2,CL2.5
TO ACCESS THE SPD =F5
ECC=N   2.90V
```

```
SPD=PC3200
ARRAY TEST @CL2->
400MHz
ARRAY TEST - OK
```

The following screens illustrates some Test Log information for DDR2 devices:

```
64Mx64`S STRUCTURE:
BANKS:1   -S:0
CHIP SIZE: 4x16Mx8
 DDR2 240P UNBUFFERED
```

```
ODT/RTT TEST:
RTT=OFF->0.262A
RTT=75 Ohm->0.858A
RTT=150 Ohm->0.555A
```

```
RTT=50 Ohm->0.858A
RTT:75=✓ 150=✓ 50=N
MODE TEST OK→
 SPEED: 400MHz
```

Basic Test Errors:

Refer to our on-line manual for additional information regarding menus .

In case of data bits error, the test halts and the defective bits are indicated as in the following message:

```
BANK 1:  DATA BITS
↔↑ B1 ✓✓✓✓✓✓FF✓ B9 ↓↔
48✓✓✓✓✓✓✓✓ F✓F✓✓✓✓✓63
16Mx72    67/150nS FPM
```

Pressing the ← or → keys allows you to examine the memory array two bytes at a time. In the above example, Bytes 7 and 8 are currently selected, and the corresponding 8 bits per byte are displayed on the next line. Pressing ↓ allows you to move down one line to examine each defective bit. The display at the bottom will then change to identify the data line corresponding to the selected bit and its pin number as indicated below:

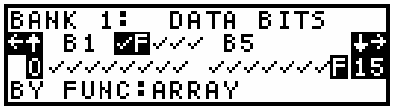
The RAMCHECK test program uses a very large number of error messages and test results. Only a small portion of them are detailed in this section. Additional error messages are

```
BANK 1:  DATA BITS
↔↑ B1 FFFF✓ B5      ↓↔
0 F✓✓FF✓✓F F✓✓FF✓✓F 15
JEDEC:DQ6   PIN=24
```

This example indicates that Byte 1 and Byte 2 are selected. Bit 7 of Byte 1 is being examined by the user as being DQ6 and being located on pin 24 of the module. Pressing ↑ allows you to move up one line and subsequently select to view the remaining bytes.

By pressing ↓ a few times, you can scroll down through more error information as discussed in Section 3.5.6. These include error address information, actual write/read pattern information, and more details about the test function type which caused the error to result:

listed on the application note section of our web site:
innoventions.com



Many other types of errors may be detected by RAMCHECK.

The following screen shows an Address Column error in address line A0 (pin 12) of Bank 1, Group 1.

We use Group1 or Group2 to describe how the memory device data bus is mapped onto RAMCHECK's internal 32-bit bus. Memory devices with 32 bits or less are directly mapped to Group1. Memory devices with 33 to 40 bits are mapped to Group1 and Group2. In Group2, bits 33 to 40 are mapped to the most significant byte. The '00000004' hex code indicates that the above address error occurred only in the third bit of group 1.

All the errors are also recorded in the Test Log, which can be viewed by pressing F4 from the STANDBY mode. The following partial sequence of two screens shows how the Test Log indicates an inconsistency in the Mode type of the various groups:

The first screen indicates the device to be FPM (Fast Page Mode) while the second screen shows that in Bank1-Group2 the mode was NIBBLE instead of FPM.

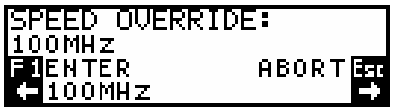
ON-THE-FLY PARAMETER CHANGES

You can change some test parameters on the fly using our "one time" override feature. Simply press F2 during the BASIC TEST to access this function, and then make the necessary selection. Because this is a "one time" change, the next memory device tested will be tested at your previous setting.

"One Time" Speed Override:

The BASIC test determines the optimized frequency (or the fastest access time) of the tested device. See Section 5 for details about the more advanced Speed Setup, which remains in effect also after you turn your RAMCHECK off.

When testing DDR or SDRAM modules, the speed override feature allows you to set a "one time" frequency override.



This kind of speed override is in effect only while the current module is tested. To set a "one time" speed override, press F2 as stated above during the BASIC test to reach the CHANGE-ON-THE-FLY screen, and then press F1 to select SPEED.

Use the ← and → keys to scroll through the available frequency rates.

When testing EDO/FPM modules, the speed override feature allows a "one time" change of nanosecond access time from RAS. Enter the speed override by pressing F2 during the Basic Test and select Speed.

Afterwards, use the ← or → to position the cursor over the current speed and then press either the ↑ or ↓ keys to increase or decrease the value. Press F1 to enter your selected speed.

Thereafter, subsequent test phases will be conducted at the selected speed, as displayed on the screen with an "@" marker.

Please note that when modules are detected as being 3V devices (e.g. SDRAM), RAMCHECK will not allow you to alter the voltage using the changed-on-the-fly feature.

Next Phase:

- If an error is detected, the defective bit(s) are identified and you can use the various error menus to examine all the details of the error. Press ESC to return to STANDBY mode. Before you press F1 to test your next device, you can press **F4** to view the Test Log of the last DUT.

- In the default RAMCHECK testflow, you cannot reach EXTENSIVE and AUTO-LOOP tests unless the BASIC TEST has been completed successfully.

- If you do not elect to terminate the test procedure after BASIC test, the following menu appears, prompting you to select the next test:

You can skip BASIC test to reach the

EXTENSIVE test for a DUT that fails BASIC test. See Section 5.

Press **F1** to go to EXTENSIVE test, **F2** to go to AUTO-LOOP. If 5 seconds pass with no user selection the EXTENSIVE test is initiated.

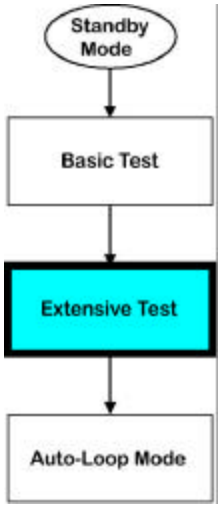
- As always, ESC terminates the test. Before you press F1 to test your next device, you can press **F4** to view the Test Log of the last tested DUT.

Significance of Successful BASIC Test:

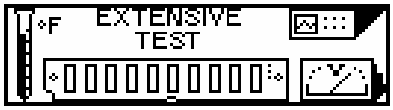
The BASIC test provides module type and speed information. It verifies that all wiring on the module is sound and that all cells in the module are operative. It also confirms basic refresh capabilities.

THE BASIC TEST IS SUFFICIENT FOR MOST SCREENING TESTS. Most defective modules will be detected during this test.

It may not detect intermittent and/or pattern sensitivity problems due to its short execution time.



4.2.3 EXTENSIVE TEST



The EXTENSIVE test is an extremely comprehensive test! Module behavior is tested under varying voltage conditions, including numerous test functions, thereby achieving a remarkably high reliability level.

What is being tested:

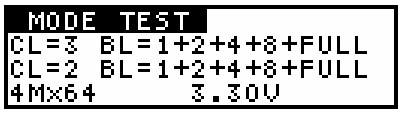
- **Voltage Cycling**: Testing under all allowable voltage conditions. These include the following ranges based on the target devices:

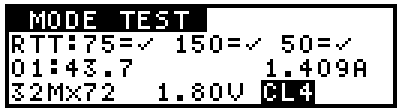
Device	Voltage Range
DDR2	1.70V – 1.95V
DDR1	2.30V- 2.70V
SDRAM	3.0V-3.6V
EDO/FPM	4.5V-5.5V or 3.0-3.6V

Please note that the actual voltage range is subject to change with product development. It depends on frequency and other parameters.

Please review our on-line manual addendum for a detailed description of the new DDR2 Mode Test.

- **Mode Test:** This phase tests the special DRAM mode of the DUT and its special features. For modern DDR2, this test includes a growing number of sub-tests for various parameters, including Burst Latency, CAS Latency, Rtt, Additive Latency and more. SDRAM mode test provides information on the module's Burst Length. Legacy DRAM technology uses two common modes: EDO and Fast Page mode. Mode failure does not halt the test, but the offending bits are shown with 'X' marks. The following screens illustrate the Mode Test results:





- **Voltage Bounce:** This phase verifies read write data retention during voltage variation. The data is written (or read) at a low voltage and read (or written) at a higher voltage. Minimal and maximal voltage levels are determined base on the type of the DUT.

Pressing F1 during the EXTENSIVE test terminates the current step and proceeds to the next one (within the EXTENSIVE test).

- **March Up/Down:** The march up/down algorithm is designed to reveal intricate problems caused by adjacent cell interference. In simplified terms, the test is done by first writing 0 to all memory locations, then, while scanning from first address to last address, the test verifies that a 0 remains in each location, then it is replaced with a 1. After the entire memory address is "marched up" in this fashion, the process reverses itself to perform the "march down" test. This time while scanning from the last address to the first address, the test verifies that a 1 remains in each location and then replaces it with a 0.

- **Relative Refresh/cell leakage:** This test provides a relative value for the ability of the memory chip to retain data between refresh cycles. "Relative" means that the result is not an absolute time value but a comparative one. Relative relation between values is exponential.
  For example: A DUT with a relative value of "5" retained data integrity twice as long as one with a value of "4" without requiring refresh. Typical good values are 3 and higher. Since this test is of the Out-of-Specification type, lower results do not imply that a module is defective, as it can still work within its published specifications!

Relative Refresh and Relatively Spikes are used only for legacy

EDO/FPM devices.

- **Relative Voltage Spikes Performance:** This test provides a relative value that indicates how well a module can sustain voltage spikes before a data loss occurs. Relative relations here are not exponential. Typical good values are 3 and above. Since this test is of the Out-of-Specification type, lower results do not imply that a module is defective, as it can still work within its published specifications!

  As you watch the red Module Power LED during the Relative Voltage Spikes test, you will see that it flashes vigorously. This LED is directly connected to the module's power supply. RAMCHECK creates artificial voltage spikes (of 5V to 1.5V or to 6.0V) after loading a complete test pattern. Memory devices with higher Relative Voltage Spikes figures can withstand more spikes in an actual application. Take into account that modules with larger built-in capacitors normally exhibit higher Relative Voltage Spikes figures due to the capacitors' smoothing effect on the spikes. Some complex modules, which utilize PAL chips and/or logic chips, may exhibit significantly lower Relative Voltage Spikes figures.

  Note that ALL relative tests are absolutely safe, as RAMCHECK DOES NOT exceed any allowable voltage/current rating!

- **Temperature stress test (Chip-Heat Mode):** In this phase, RAMCHECK tests memory chips at the actual higher operation temperature experienced inside a computer. Being able to test at the proper temperature is extremely important because some memory problems are not exhibited until the chip is warmed up. As the mode progresses, you will note that RAMCHECK will display the heating current in Ampere units.

The EXTENSIVE test display shows the current test type, duration of test, applied voltage, Access Time (speed in nanoseconds or frequency rate), and module mode type and size. The final test results look similar to those of the BASIC test. Note that because the DUT is tested at a higher temperature during the Chip-Heat portion of the EXTENSIVE test, the Access Time might be slower than the value obtained with the BASIC test.

Next Phase:

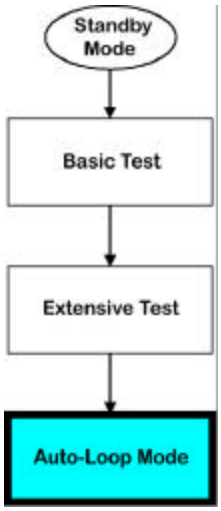
- If an error is detected during the EXTENSIVE test, the defective bit(s) are identified and the display waits for your acknowledgment. Press ESC after review to return to Standby Mode.

- If no errors are detected - an OK test result is shown and you are prompted to continue. Press F1 to go to AUTO-LOOP for burn-in and pattern tests. If the time delay passes with no user selection, the AUTO-LOOP test is initiated.

- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

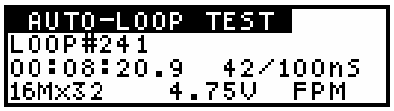
Significance of Successful Test:

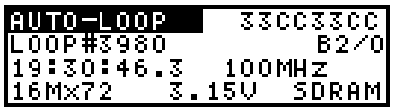
The EXTENSIVE test verifies proper module operation under varying voltage conditions. It will detect intermittent problems which are either temperature dependent or resulting from adjacent cell interference. It provides comparative scores of module performance. It further tests the module with additional data patterns besides those utilized by the BASIC test.

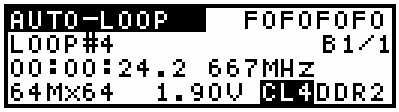


4.2.4 AUTO-LOOP TEST

During the AUTO-LOOP test, the module is endlessly tested with different patterns of data bits, generated by different algorithms.



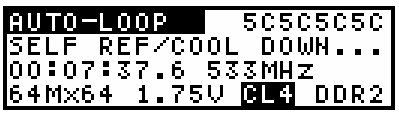




AUTO-LOOP is an excellent burn-in procedure, as it will continue indefinitely until the user presses the Esc key. The time of the test, the iteration (loop) number, applied voltage, module speed and cycle time, module size, and mode type are displayed.

A recommended Calibration & Upgrade procedure is available from

Some long tests like Self Refresh are incorporated into AUTO LOOP as shown in the following screen:



Next Phase: The AUTO-LOOP test terminates when an error is

the factory. Refer to Appendix H in the enclosed CD for details.

detected or in response to the user's command.

- If an error is detected, the defective bit(s) are identified and the display waits for your acknowledgment.
- If no error is detected, the test will continue indefinitely; or until ESC is pressed to terminate the test. As the tester and module may get hot, make sure the test area is well ventilated (see Safety Precautions).

- As always, ESC terminates the test. Before you press F1 to test your next device, you can press F4 to view the Test Log of the last tested DUT. The Test Log provides you with a detailed list of all the test results, including speed drift information.

Significance of a Successful Test:

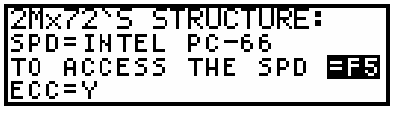
AUTO-LOOP is designed to detect pattern sensitivity problems, as it tests the modules under many different patterns. 20 minutes or more are sufficient to detect most pattern sensitivity problems.

Notice that the AUTO-LOOP mode makes RAMCHECK an excellent instrument for continuous burn-in procedure.

4.4 SPD MANAGEMENT

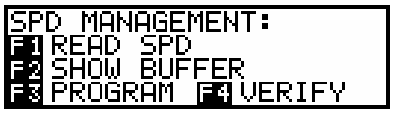
The SPD (Serial Presence Detect) is a small 8-pin EEPROM chip mounted on DIMMs & SO DIMMs that includes vital information about the module's parameters.

You can access the SPD Management Mode from Standby Mode by pressing F4, F3. You can also enter this mode after the Basic Test has begun by pressing F5, F3, and F5. At the conclusion of the Basic Test, the final summary screen will give you the option to access the SPD Management Mode once again.



This example shows results obtained with an SDRAM DIMM. RAMCHECK indicates if the SPD device is programmed to show module compliance with the Intel PC-66, PC-100, or PC-133.

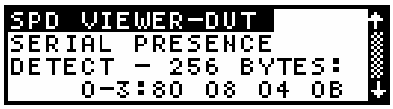
If you choose not to view the SPD, do nothing, and the test flow will continue as normal. Choosing to view the SPD of the device (by pressing F5) will terminate the test flow and display the SPD management screen.

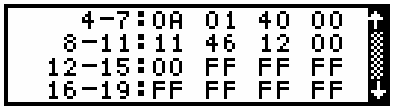


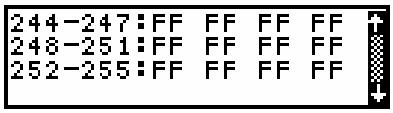
RAMCHECK's SPD Management mode is the operational mode to read and program SPD data.

READ SPD

Press F1 to read the current module's SPD and keep this information in RAMCHECK's buffer. The SPD viewer displays information in a multipage list format. Use the ↑ and ↓ keys to scroll between the pages. The following screen images show a partial view of the SPD codes for a typical DIMM.







In the above examples, byte 0 contains "80", byte 1 contains "08", byte 5 contains "01", and byte 9 contains "46". You will also note that bytes 244 through 255 contain "FF"; this is an indication that these bytes are not being used.

RAMCHECK's buffer will retain this SPD information until:

a) new SPD data is read;
b) an SPD file is downloaded from the PC Downloader;
c) your RAMCHECK is turned off.

SHOW BUFFER

Use SHOW BUFFER to view the current contents of RAMCHECK's buffer without reading the SPD of a module installed in the tester. This allows you to view the buffer after an SPD file download, or after reading the SPD of a module.

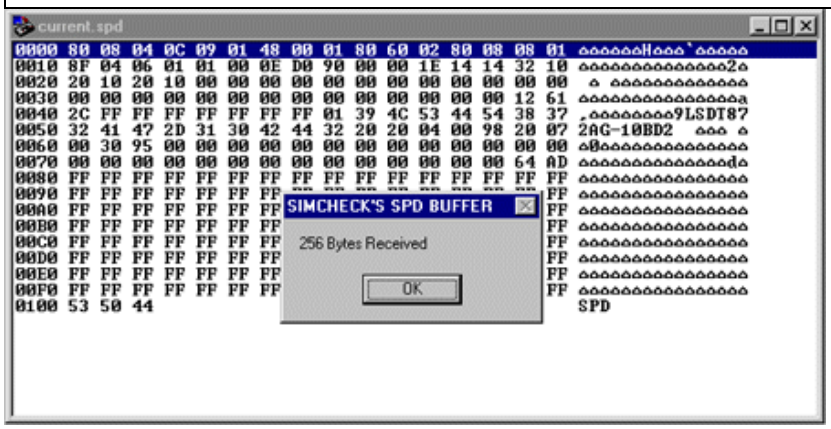
Please refer to Section 6. for further details.

SPD EDITING AND FILING

When RAMCHECK communicates with the PC Program Software, you can further read SPD data into the PC, edit the data on your PC screen, save it into *.spd files on your PC, or download stored SPD files into RAMCHECK's buffer for programming other modules.

NOTE: When viewing information on the PC Screen, the SPD data, as well as the address locations, are displayed in hexadecimal format.

When viewing the information on RAMCHECK's LCD display, the address locations are displayed in decimal format, while the SPD data values remain in hex.



RAMCHECK BUILT-IN SPD BYTE EDITOR

The stand-alone quick byte editor (included with RAMCHECK firmware version 2.19 and higher) allows advanced users to change and program SPD data without the need to interface the RAMCHECK to a PC.

While the RAMCHECK is in standby mode, press F4, then press **F3** for "SPD Management". Insert the memory device with the SPD to be changed into the test socket. Press **F1** to "Read Buffer" to transfer the information from the SPD chip of the memory device to the RAMCHECK's internal memory, pressing **F4**/**F3** will scroll through the SPD data. (Note: The byte locations are in decimal, not HEX as in the PC Communications software.) Once you have finished reviewing the data, press the ESC key to go back to the menu.

Next press **F5** for "EDIT", using **F2**/**F5** to move the cursor and **F3**/**F4** to enter the byte location (in decimal) you want to change, then press **F1**. Use **F2**/**F5** to move the cursor and **F3**/**F4** to change the desired value in HEX. Next, press **F2** for "Show Buffer", using **F4**/**F3** to scroll through the data to confirm that the byte location you change earlier has been change. Next, press the ESC key and then press **F3** to "Program". Next, press **F4** for "Verify" to make sure the SPD data in the RAMCHECK's internal memory matches the SPD data just programmed in the SPD chip on the memory device. If it flashes "OK" then you have successfully program the SPD with the change. If you want to program another byte location repeat the steps above.

SPD PROGRAMMING

SPD programming should only be done by manufacturers and individuals that are well familiar with SPD data; therefore we

recommend that these features only be performed by advanced users, as programming a DIMM module's SPD with erroneous data will render the module inoperable!!!

Use **F3** to program the data in the buffer into the SPD on the inserted DIMM module. To avoid casual users from programming wrong SPD data, the default SPD setting in your RAMCHECK is to have SPD programming disabled:

```
PROGRAMMING DISABLED!
USE SETUP-CONFIG-SPD
```

You may enable SPD programming from Standby Mode by entering the following key sequence:

F2 Enters Setup Mode
F3 Enters CONFIG. Menu
F4 MORE
F3 SPD

A warning screen will appear indicating that this function is for advanced users only. After a small time delay, the SPD Programming menu appears (Press F1 if you wish to bypass this time delay in the future). Select the F2 key to enter Programming Mode,

```
SPD PROGRAMMING

F1 ENTER        ABORT Esc
 ← DISABLED             →
```

PLEASE REFER TO SECTION 5.5.6 FOR AN EXPLANATION OF PROGRAMMING MODES.

Use the right arrow button to select the programming mode. Press F1 to enter your selection. Press the ESC key a few times to return to Standby Mode.

Remember that you must have a valid SPD file in the RAMCHECK buffer (use SHOW BUFFER to make sure) before you start programming. Press F3 from the SPD Management Mode Menu to program your SPD. RAMCHECK programs the SPD and verifies the data with an OK (or fail) message at the bottom of your screen:

```
PROGRAMMING...
(16-BYTE PAGE) ****

   OK
```

VERIFY

The VERIFY function (F4) compares the actual SPD data on the inserted DIMM module with RAMCHECK's internal buffer. This will either indicate OK if the data matches, or FAIL if the data is different.

PRODUCTION MODE

The Production Mode is a special SPD programming setup whereby

the SPD of the module being tested is programmed immediately following the test.

This setup is for advanced users only. Those wishing to setup the production mode may acquire further details from our Application Note listed in the Tech Support section of our website (www.innoventions.com).

For a much more in-depth look at RAMCHECK SPD support, please refer to the addendum in section 6.3 SPD Support.

4.5 RAMCHECK DDR PRO ADAPTER

The RAMCHECK line extends its comprehensive support for testing the high speed DDR DIMM modules using the RAMCHECK DDR PRO Adapter (p/n INN-8668-9). This manual addendum describes the operation of this adapter as well as the DDR S.O. DIMM Converter.

OPERATION

This adapter connects to RAMCHECK via the two top 90-pin and 50-pin expansion slots. Turn RAMCHECK OFF and carefully mount the adapter onto RAMCHECK expansion slots, while pressing it gradually on both sides.

CAUTION: Plug this adapter into the expansion slots only when RAMCHECK is OFF! Failure to turn RAMCHECK OFF when connecting or disconnecting the DDR PRO Adapter may result in damage to the internal PAL chips of both the RAMCHECK and the Adapter!

While the DDR Pro adapter is installed on RAMCHECK, you can test **only** the 184-pin DDR modules. To test the 168-pin DIMM modules the adapter must be removed. First turn the RAMCHECK OFF and carefully remove the DDR PRO adapter by gradually pulling it up on both sides, taking care not to flex the adapter's boards.

CAUTION: Please let the adapter **COOL DOWN** for at least 1 minute before attempting to remove it from RAMCHECK. Removal of the adapter while hot may impair some soldered connections of its delicate internal parts!

RAMCHECK automatically recognizes the presence of the DDR PRO Adapter with the following turn-on screen:

Required RAMCHECK Firmware Version: 2.23E or later.

DDR DIMM HANDLING

The DDR PRO Adapter supports 184-pin DDR DIMM modules.

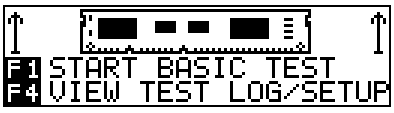
INSERTION: The DDR PRO Adapter uses a vertically mounted high quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DDR DIMM into the socket, pushing it evenly along its top. Pin 1 of the module should point to the left side (as marked on the adapter), so that the key area of the module's connector is correctly aligned with the key area in the test socket. When the DIMM is properly inserted, the ejectors will snap onto the half circle notches on each side of the module.

REMOVAL: The DIMM is easily released from the socket by pulling both ejectors sideways.

NOTE: DIMM insertion and removal should be done only when RAMCHECK is in STANDBY Mode. The RED "Module Power" LED should be OFF in STANDBY mode.

DDR DIMM TESTING

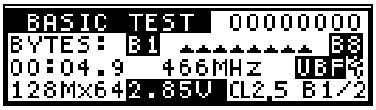
Turn RAMCHECK ON once the DDR PRO Adapter is installed and insert the first DIMM module. There is no need for special setup with RAMCHECK since it automatically recognizes the DDR adapter. When RAMCHECK enters the STANDBY mode, the display will prompt you to test DDR modules.



The DDR test procedure is initiated by pressing the F1 key and is designed to follow the regular RAMCHECK test flows. Unless your press the ESC key, EXTENSIVE TEST follows BASIC TEST, and AUTO-LOOP follows BASIC TEST.

DDR BASIC TEST

The DDR PRO allows you to set up various test parameters like the voltage, the test frequency, and the choice of a CAS Latency. This screen shows user selected voltage setup of 2.85V.



At the start of Basic Test, RAMCHECK provides power and proper initialization sequence (involving control and clock lines) to the DDR module. A large variety of quick wiring tests are conducted, the module structure and frequency is determined, and the memory array tests begin. Since the wiring and structure tests are extremely fast, their results are logged in the Test Log and reported after the end of Basic Test, unless an error is encountered. In the default mode, the test runs through two main phases - it starts with CL=2 and follows with CL=2.5.

Before discussing the wiring and structure test results, let us review the two main phases of the Basic Test, the memory array tests at two different CAS Latencies (CL=2 and CL=2.5 by default). These array tests take the bulk of the time of the Basic Test.

Memory Array Test at CL=2

The following screen shows the information provided during the first main phase of Basic Test - the array test for CL=2:

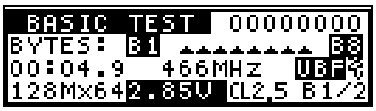
In this example, a 32Mx64 Unbuffered (marked UBF) module is tested at CL=2 at 400MHz. The entire memory array is written and verified twice to catch most memory cell stuck problems. The marker to the right of the UBF message indicates that the test is set at STTL 2.5V. However, the actual voltage is automatically adjusted to 2.70V (as shown in the screen) for modules running at 400MHz or faster. You can use setup or change-on-the-fly to set up your own fixed voltage selection.

The "B1/1" marker at the bottom right corner is the "section under test" indicator, which has been modified for DDR devices. With DDR devices, each chip has four internal banks, which are selected by the BA1 and BA0 bank address lines. The module itself may have one or two main banks which are selected by S0 and S1 control lines. In this example, "B1/1" indicates that the section under test is the module's first main bank (also known as rank) and the internal chips bank 1. If the marker was "B1/0", it would indicate main bank 1 and internal chips bank 0. A "B2/3" marker indicates the second main bank (rank #2) and internal chips bank 3. Similarly, "B1/2" would indicate main bank 1 and internal chips bank 2, and so on. Modules with only one main bank will scan "B1/0"->"B1/1"-> ... ->"B1/3", before switching to the next test pattern. Modules with two main banks will scan "B1/0"-> ... ->"B1/3"->"B2/0"->...->"B2/3" for each test pattern.

Please note that a 400MHz module may legitimately drop in speed during the more stringent CL2 CAS LATENCY array test. Similarly, a 266Mhz module may drop to 233Mhz or 200Mhz (a 333MHz module to 300Mhz or 266MHz) during the CL2 array test.

Memory Array Test at CL=2.5

After the completion of the first memory array test at CL=2, the second memory array test at CL=2.5 is conducted.

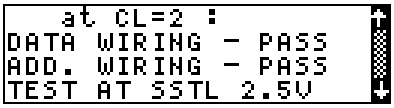


In this example (using a different module for the screen capture), a 128Mx64 Unbuffered module is tested at 466MHz and at CL=2.5. If testing Registered modules, the screen will look like this:

Registered modules are marked by the "REG" reversed message. In the above screen, a 32Mx72 Registered module is set up at 333Mhz. Please note that the test voltage defaults to 2.50V at such frequency.

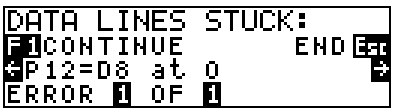
Wiring tests at the start of the Basic Test

At the start of the Basic Test, RAMCHECK performs a large number of wiring tests to verify that data lines, address lines and control lines are properly wired and function.

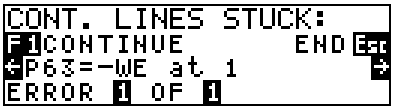


If no wiring problems are detected, the above screen is written into the Test Log. In the event of errors, RAMCHECK stops the test and provides error indication as well as detailed information regarding the pin connection associated with the detected error. Error report styles are similar to other RAMCHECK error reports for SDRAM and EDO/FPM devices.

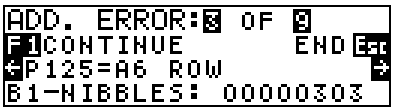
The following screens provide some examples:



The above screen shows data line D8 (connector pin-12) stuck at logic '0'.



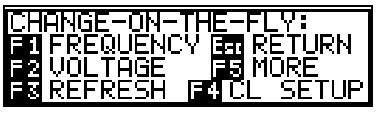
The above screen shows control line -WE (connector pin-63) stuck at logic '1'.



This address error example indicates an error in row address line A6 (connector pin 125) which affect some portion of the individual chips of the module. Since all address lines multiplex both rows and columns, an address error may affect ROW, COL (column) or ROW+COL. The bottom line further shows which data bits in the current bank are affected by the detected error. This allows an advanced user (e.g. a memory technician who can repair the module) to identify individual defective chips on the module. All DQ lines are divided into 4-bit groups called NIBBLES, and the hex number indicate which nibbles are affected by the address errors. In the above example, the nibbles code ...0303 is translated to ... 01100000011, indicating problems in nibbles 0,1,8 and 9.

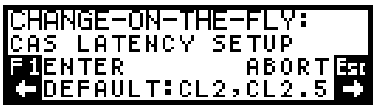
Change-On-The-Fly of Basic Test

RAMCHECK provides a rich sets of parameters that can be changed during the Basic Test. We distinguish the Change-On-The-Fly setup which affects ONLY the current test from the "permanent" Setup which controls the test parameters, unless changed by the user. For example, if you setup the frequency to 400MHz, then all tests will be fixed at 400MHz. If you run Basic Test and use the Change-On-The-Fly to set the frequency to 400MHz, then the current test will run at 400Mhz but subsequent tests will run at the regular default frequencies (or "permanent" setup frequencies). To reach the Setup menu, press F2 during Standby mode. To activate the Change-On-The-Fly, first start Basic Test and then press F2. The following main menu will appear:



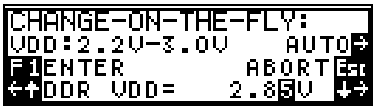
Any change done via the Change-On-The-Fly menu is relevant during the current test. Permanent setup changes can be done via the regular Setup menu, which is activated by pressing F2 during STANDBY.

Expanded CHANGE-ON-THE-FLY can be used to set up the Frequency, the Voltage, the CAS LATENCY and the Refresh rate only for the current test. Following the test, it returns to the current setup parameters.



The DDR PRO allows you to set up the CAS LATENCY. This screen shows our default setup which allows the test program to selected CL=2 or CL=2.5 during each test phase.

In this example, the CAS LATENCY was fixed to CL=2.5 throughout the tests. Similarly, CAS Latency can be set to CL3, CL2.5, where the test starts with CL3 and follows with CL2.5. Also, you can select CL2 ONLY or CL3 ONLY.

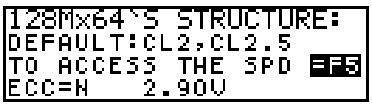


The new DDR PRO VDD Voltage setup allows the user to change on-the-fly the test voltage in the range 2.2V-3.0V. When set to AUTO, RAMCHECK automatically tests the module at 2.5V/2.7V.

Basic Test Results

The following screen shows the first summary screen following a successful Basic Test with another module:

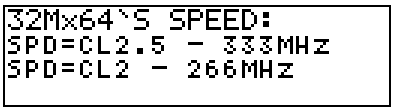
In this example, a DDR 512MB module, organized as 64Mx64 was tested at 266MHz. The module was of the Unbuffered type (UBF message), tested at 2.5V (like all DDR devices), and it uses 3 differential clock pairs.



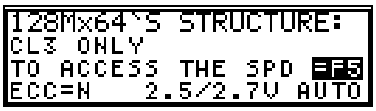
RAMCHECK Basic Test provides several screens for test results. The third structure screen shown here includes some of the new features of the DDR PRO, including the CAS LATENCY and the voltage setup.

During the Basic Test, RAMCHECK tests the operation of the three Burst Length available in DDR devices - 2, 4, and 8. Unlike older SDRAM, new DDR devices do not support Full Page Burst. The following screen shows a summary screen indicating that BL (Burst Length) was tested OK:

During the Basic Test, RAMCHECK interrogates the SPD of the module to read the maximum declared frequency at CAS LATENCY (CL) 2 and 2.5:



The above example shows the reading from a typical PC2700/PC333 module. Such a module can reach 333MHz operation only in the slower CL2 mode.



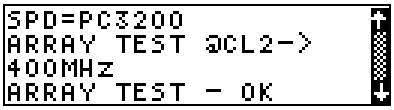
Here is another example where the CAS LATENCY was set at CL3 ONLY and the voltage left at automatic mode (2.5V for modules running up to 333MHz, 2.7V for higher speed modules).

RAMCHECK Test Log

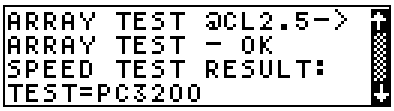
The RAMCHECK Test Log allows you to review all the test results in one continuous scrolling display. You can view the test even after the test ends (but before you start a new test) by pressing F3 from Standby and selecting Test Log with F1. The following screens show you some of the new features of the DDR PRO adapter as seen in the Test Log.

RAMCHECK's built in test log shows the actual voltage of the test.

CAS LATENCY override is shown in the Test Log. In this example, the module is tested at CL=3 only. In the automatic (default) mode, the CAS LATENCY is changed between CL=2 and CL=2.5



This screen shows the speed to be 400MHz during the CL2 test array portion of the test. **Please note that a 400MHz module may legitimately drop in speed during the more stringent CL2 CAS LATENCY array test.**.



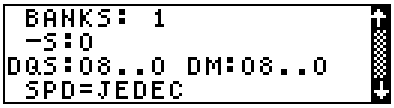
This screen shows second array test portion of Basic Test, which is run at CL2.5. User can also select CL2 or CL3 or CL2.5 ONLY test.

Module's use of DQS and DM control lines

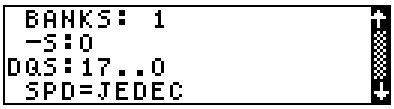
DDR memory devices use data read/write strobe signals (DQS) as well as Data Mask (DM) signals for masking write activity on the selected chip. The DQS line controls the transfer of data from and to the memory device. When the DM signal is set high, the attached DDR device will not accept data which is written to it, that is, the written data is masked out from changing the memory device contents. The 184-pin connector includes either 9 DQS line and 9 DM lines or only 18 DQS lines.

Most DDR module are made of x8 type DDR chips and they are wired to use 9/8 DQS lines (9 for x72 ECC DIMMs, only 8 for x64 DIMMs). They

also use 9/8 DM lines. Such modules are identified in RAMCHECK's Test Log with the line "DQS:08..0 DM:08..0" as depicted in the following screen:



Some Registered modules which are made of x4 type DDR chips are wired to 18/16 DQS lines (18 for x72 ECC DIMMs, only 16 for x64 DIMMs). The DM control line of the DDR chips of such modules are disabled by a fixed connection to ground. Such modules are identified in RAMCHECK's Test Log with the line "DQS:17..0" as shown in the following screen:



Some examples for modules with 18 DQS control lines include Samsung p/n M383L6420DTS and Micron Technology p/n MT18VDDT3272G.

DDR Parameters Setup

You can permanently change test parameters using RAMCHECK Setup Menu. You reach Setup by pressing F2 from Standby mode. Press F1 to select Parameter Setup. Setup parameter menus are similar to the Change-On-The-Fly menus discussed above. The following screen shows the DDR Voltage Setup:

Unlike the CHANGE-ON-THE-FLY above where the new voltage setup is effective for one test, you can use the Setup Parameters to change the test voltage parameters for all tests.

DDR EXTENSIVE TEST

The EXTENSIVE TEST for DDR is similar to our regular SDRAM test. Currently, the following test phases are performed:

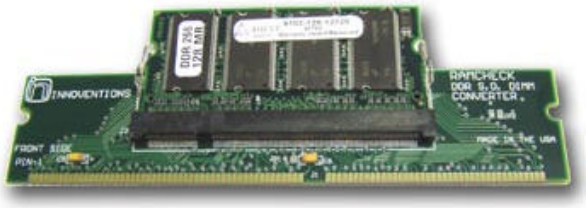
- Voltage Cycling
- Voltage Bounce
- March Up/Down
- Chip Heat
- Final Test

AUTO-LOOP TEST

The AUTO-LOOP test uses changing patterns to burn-in the module and to detect cell interferences.

4.6 RAMCHECK DDR S.O. DIMM CONVERTER

The DDR S.O. DIMM Converter (p/n INN-8668-6-1) allows testing of 200-pin DDR S.O. DIMM (PC333/266/200) on the DDR-184-pin Adapter (p/n INN-8668-6).



The converter is made in the shape of a standard 184-pin DIMM module, but without the center key. It has special electronics for RAMCHECK's auto-detection, and it is designed for low noise and short signal connections.

OPERATION

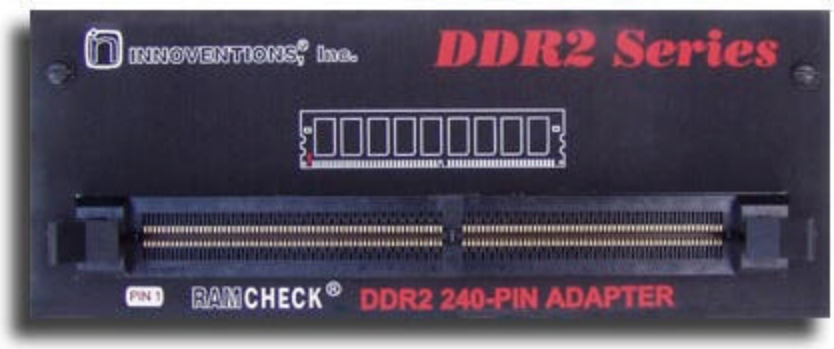
Place the converter on a flat surface that is covered with a proper anti-static sheet. Insert the 200-pin SO DIMM into socket J2, making sure that the module's pin-1 is facing left. Socket J2 is similar to the standard laptop sockets, and it has metal latch to insure proper retention of the module in place. We have selected the AMP gold plated sockets as the best available in the market. Once inserted, the module surface locks in parallel to the converter board, with the module's front side aligning with the converter's front side.

Insert the converter into the DDR adapter's 184-pin test socket as if it was a regular DDR module, making sure that pin-1 faces left. Press F1 to start the test, which generally follows the regular DDR test flow as outlined above.

At the end of the test (RED power LED must be off), remove the converter and place it on the protected flat surface for removal of the tested S.O. DIMM module.

The converter is auto detected, and RAMCHECK's standby message should continue to indicate a 200-pin S.O. DIMM until a regular 184-pin DDR module is tested.

4.7 RAMCHECK DDR2 ADAPTER



The RAMCHECK DDR2 240-Pin Adapter (p/n INN-8668-12) is for testing modern DDR2 DIMMs.

NOTE: You must have Firmware Version 2.33 or higher to support the new DDR2 Adapter.

OPERATION

This adapter connects to RAMCHECK via the two top 90-pin and 50-pin expansion slots. Turn RAMCHECK OFF and carefully mount the DDR2 adapter onto the RAMCHECK expansion slots, while pressing it gradually on both sides.

CAUTION: Plug this adapter into the expansion slots only when RAMCHECK is OFF! Failure to turn RAMCHECK OFF when connecting or disconnecting the DDR2 Adapter may result in damage to the internal chips of both the RAMCHECK and the Adapter!

While the DDR2 adapter is installed on RAMCHECK, you can test only the 240-pin DDR2 modules. To test the 168-pin DIMM modules, the DDR2 adapter must be removed. First turn the RAMCHECK OFF and carefully remove the DDR2 adapter by gradually pulling it up on both sides, taking care not to flex the adapter's boards.

CAUTION: Please let the adapter COOL DOWN for at least 1 minute before attempting to remove it from RAMCHECK. Removal of the adapter while it is still hot may impair some of the soldered connections of its delicate internal parts!

RAMCHECK automatically recognizes the presence of the DDR2 Adapter with the following initial turn-on screen:

Required RAMCHECK Firmware Version: 2.33 or later.

DDR2 DIMM HANDLING

The DDR2 Adapter supports the 240-pin DDR DIMM modules.

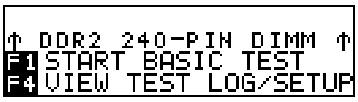
INSERTION: The DDR2 Adapter uses a vertically mounted high quality test socket with two ejectors that need to be opened prior to insertion. Carefully insert the DDR2 DIMM into the socket, pushing it evenly along its top. Pin 1 of the module should point to the left side (as marked on the adapter), so that the key area of the module's connector is correctly aligned with the key area in the test socket. When the DIMM is properly inserted, the ejectors will snap onto the half circle notches on each side of the module.

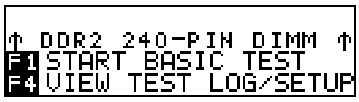
REMOVAL: The DIMM is easily released from the socket by pulling both ejectors sideways.

NOTE: DIMM insertion and removal should be done only when RAMCHECK is in STANDBY Mode. The RED "Module Power" LED should be OFF in STANDBY mode.

DDR2 DIMM TESTING

Turn RAMCHECK ON once the DDR2 Adapter is installed. There is no need for special setup with RAMCHECK since it automatically recognizes the DDR2 adapter. When RAMCHECK enters the STANDBY mode, the display will prompt you to test DDR2 modules. Insert the DIMM module.





The DDR2 test procedure is initiated by pressing the F1 key and is designed to follow the regular RAMCHECK test flows. Unless your press the ESC key, EXTENSIVE TEST follows BASIC TEST, and AUTO-LOOP follows EXTENSIVE TEST.

DDR2 BASIC TEST

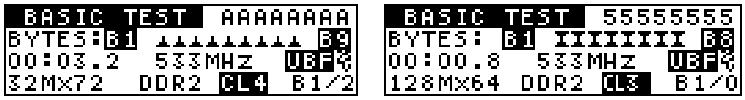
The DDR2 Adapter allows you to set up various test parameters like the voltage, the test frequency, and the choice of a CAS Latency. The following screen previews the BASIC TEST, showing a user-selected CAS Latency of 4.

At the start of BASIC TEST, RAMCHECK provides power and proper initialization sequence (involving control and clock lines) to the DDR2 module. A large variety of quick wiring tests are conducted, the module structure and frequency is determined, and the memory array tests begin. Since the wiring and structure tests are extremely fast, their results are logged in the Test Log and reported after the end of BASIC TEST, unless an error is encountered.

Before discussing the wiring and structure test results, let us review the main phase of the BASIC TEST, the memory array test RAMCHECK uses CL=3 for the for modules below 533MHz, and CL=4 or more for modules running at 533MHz or higher. You can use setup in the Change-on-the-Fly feature to control the CL setting. These two array tests take the bulk of the time of the BASIC TEST.

The Memory Array Test

In its default setup, RAMCHECK selects CL=3 for modules that run below 533MHz and CL=4 for modules running at 533MHz or above. You can override the CL setup. The following screens show the information provided during the first main phase of the BASIC TEST with a typical PC3200 module which defaults to CL=3:



In the left example, a 32Mx72 unbuffered (marked UBF) module is tested at CL=4 at 533MHz. The entire memory array is written and verified twice to catch most "memory cell stuck" problems. The marker to the right of the UBF message indicates that the test is set at STTL 1.8V. However, the actual voltage is automatically adjusted to 1.90V for modules running at 533MHz or higher. You can use setup or change-on-the-fly to set up your own fixed voltage selection. The two screens alternate during the test so that you can see the test voltage.

The "B1/0" marker at the bottom right corner is the "section under test" indicator, which has been modified for DDR2 devices. With DDR2 devices, each chip has four internal banks, which are selected by the BA1 and BA0 bank address lines. The module itself may have one or two main banks which are selected by S0 and S1 control lines. In this example, "B1/0" indicates that the section under test is the module's first main bank (also known as rank) and the internal chips bank 0. If the marker was "B1/1", it would indicate main bank 1 and internal chips bank 1. A "B2/3" marker indicates the second main bank (rank #2) and internal chips bank 3. Similarly, "B1/2" would indicate main bank 1 and internal chips bank 2, and so on. Modules with only one main bank will scan "B1/0"->"B1/1"-> ... ->"B1/3", before switching to the next test pattern. Modules with two main banks will scan "B1/0"-> ... ->"B1/3"->"B2/0"->...->"B2/3" for each test pattern.

Some modules cannot run at CL=3, or are setup by the user to test at CL=2. The following screen shows the information provided during an array test at CL=2:

In this example, a 64Mx64 Unbuffered (marked UBF) module is tested at CL=2 at 400MHz.

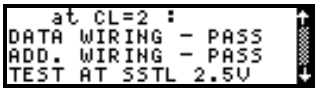
Please note that a 667MHz or 533MHz modules may legitimately drop in speed during the more stringent CL2 CAS LATENCY array test.

In this example (using a different module for the screen capture), a 128Mx72 Unbuffered module is tested at 400MHz and at CL=2. If testing Registered modules, the screen will look like this:

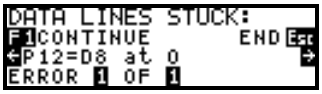
Registered modules are marked by the "REG" reversed message. In the above screen, a 128Mx72 Registered module is set up at 533Mhz. Please note that the test voltage defaults to 1.90V at such frequency.

Wiring tests at the start of the Basic Test

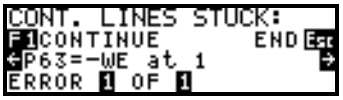
At the start of the Basic Test, RAMCHECK performs a large number of wiring tests to verify that data lines, address lines and control lines are properly wired and function.



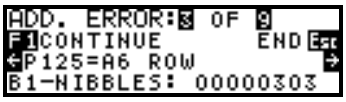
If no wiring problems are detected, the above screen is written into the Test Log. In the event of errors, RAMCHECK stops the test and provides error indication as well as detailed information regarding the pin connection associated with the detected error. Error report styles are similar to other RAMCHECK error reports for SDRAM and EDO/FPM devices. The following screens provide some examples:



The above screen shows data line D8 (connector pin-12) stuck at logic '0'.



The above screen shows control line -WE (connector pin-63) stuck at logic '1'.



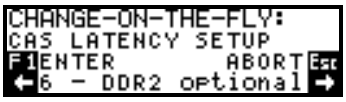
This address error example indicates an error in row address line A6 (connector pin 125) which affects some portion of the individual chips of the module. Since all address lines multiplex both rows and columns, an address error may affect ROW, COL (column) or ROW+COL. The bottom line further shows which data bits in the current bank are affected by the detected error. This allows an advanced user (e.g. a memory technician who can repair the module) to identify individual defective chips on the module. All DQ lines are divided into 4-bit groups called NIBBLES, and the hex numbers indicate which nibbles are affected by the address errors. In the above example, the nibbles code ...0303 is translated to ... 01100000011, indicating problems in nibbles 0,1,8 and 9.

Change-On-The-Fly for the Basic Test

RAMCHECK provides a rich set of parameters that can be changed during the BASIC TEST. We distinguish the Change-On-The-Fly setup which affects ONLY the current test from the "permanent" setup which controls the test parameters, unless changed by the user. For example, if you set up the frequency to 400MHz, then all tests will be fixed at 400MHz. If you run BASIC TEST and use the Change-On-The-Fly to set the frequency to 400MHz, then the current test will run at 400Mhz but subsequent tests will run at the regular default frequencies (or "permanent" setup frequencies). To reach the Setup menu, you press F2 during Standby mode. To activate the Change-On-The-Fly, you must first start BASIC TEST and then press F2. The following main menu will appear:

Any change done via the Change-On-The-Fly menu is relevant during the current test. Permanent setup changes can be done via the regular Setup menu, which is activated by pressing F2 during STANDBY.

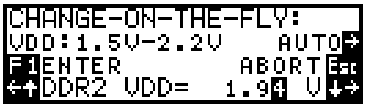
The DDR2 Adapter allows you to set up the CAS LATENCY:



In this example, the CAS LATENCY was fixed to CL=6 throughout the

tests. DDR2 supports CL of 3,4, and 5. They may optionally support CL of 2 and 6, as shown in this example.

Voltage Setup

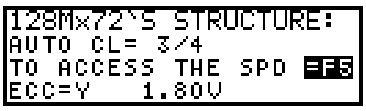


The new DDR2 VDD Voltage setup allows the user to change on-the-fly the test voltage in the range 1.5V-2.2V. When set to AUTO, RAMCHECK automatically tests the module at 1.8V/1.9V.

Basic Test Results

The following screen shows the first summary screen following a successful Basic Test with another module:

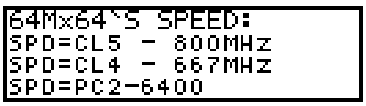
In this example, a DDR2 1GB module, organized as 128Mx72, was tested at 400MHz. The module was of the Unbuffered type (UBF message), tested at 1.8V (like all DDR2 devices), and it uses 3 differential clock pairs.



RAMCHECK Basic Test provides several screens for test results. The third structure screen shown here includes some of the new features of the DDR2, including the CAS LATENCY and the voltage setup.

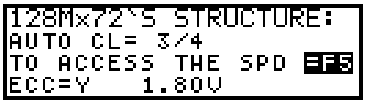
During the Basic Test, RAMCHECK tests the operation of the two Burst Lengths available in DDR2 devices - 4 and 8. Unlike older SDRAM, new DDR2 devices do not support burst length of 2 and Full Page Burst. The following screen shows a summary screen indicating that BL (Burst Length) was tested OK:

During the Basic Test, RAMCHECK interrogates the SPD of the module to read the maximum declared frequency as based on the various CL settings:



The above example shows the reading from a PC2-6400 DDR2 module.

Such a module can reach 667MHz at CL4 and 800MHz at CL5. The adapter tests this module at a maximum of 667MHz. All other PC2-5400/4200/3200 are tested at the maximum indicated speed.

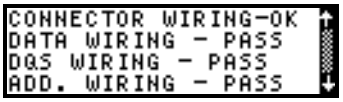


Here is another example where CAS LATENCY was set automatically to 3 or 4 depending on the test frequency. The example also includes an ECC DDR2 module and the test voltage was maintained at 1.8V.

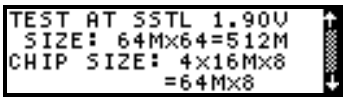
RAMCHECK Test Log

The RAMCHECK Test Log allows you to review all of the DDR2 test results in one continuous scrolling display. You can view the test even after the test ends (but before you start a new test) by pressing F3 from Standby and selecting Test Log with F1. The Test Log is one of RAMCHECK's most powerful features. When used with the PC Communications program, the test log can be printed and saved into convenient log files.

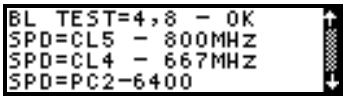
The following screens show you some of the new features of the DDR2 adapter as seen in the Test Log.



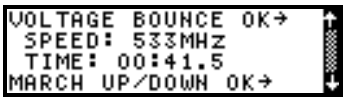
Numerous wiring tests are executed at the start of Basic Test. This screen illustrates some of these results in the Test Log.



This screen shows the detailed structure of the chip comprising the DDR2 module. It also indicates the actual test voltage.



This screen shows the SPD marking of the module speed at CL5 and CL4. Please note that the module's maximum speed may legimately drop in speed during the more stringent CL array tests..

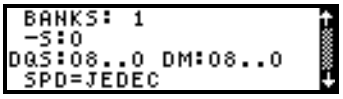


This screen demonstrates that the results from the DDR2 Extensive Test. The Voltage Bounce test has been completed successfully.

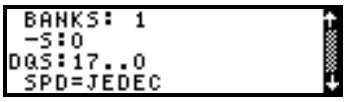
DDR2 Module's use of DQS and DM control lines

DDR2 memory devices use data read/write strobe signals (DQS) as well as Data Mask (DM) signals for masking write activity on the selected chip. The DQS for DDR2 come as a differential pairs, and they control the transfer of data from and to the memory device. When the DM signal is set high, the attached DDR2 device will not accept data which is written to it, that is, the written data is masked out from changing the memory device contents. The 240-pin connector includes either 9 pairs of DQS lines and 9 DM lines or only 18 pairs of DQS lines. The DDR2 adapter set the DQS pairs in accordance with the differential SSTL1.8 standard. Some tests can set the DDR2 devices for single DQS lines.

Most DDR2 modules are made of x8 type DDR chips and they are wired to use 9/8 DQS lines (9 for x72 ECC DIMMs, only 8 for x64 DIMMs). They also use 9/8 DM lines. Such modules are identified in RAMCHECK's Test Log with the line "DQS:08..0 DM:08..0" as depicted in the following screen:

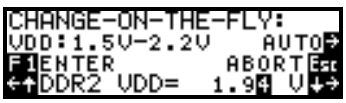


Some Registered modules which are made of x4 type DDR2 chips are wired to 18/16 DQS lines (18 for x72 ECC DIMMs, only 16 for x64 DIMMs). The DM control line of the DDR2 chips of such modules are disabled by a fixed connection to ground. Such modules are identified in RAMCHECK's Test Log with the line "DQS:17..0" as shown in the following screen:



DDR2 Parameters Setup

You can permanently change test parameters using the RAMCHECK Setup Menu. You reach Setup by pressing F2 from Standby mode. Press F1 to select Parameter Setup. Setup parameter menus are similar to the Change-On-The-Fly menus discussed above. The following screen shows the DDR Voltage Setup:



Unlike the CHANGE-ON-THE-FLY above where the new voltage setup is effective for one test, you can use the Setup Parameters to change the test voltage parameters for all tests.

DDR2 EXTENSIVE TEST

The EXTENSIVE TEST for DDR2 is similar to our DDR1 and SDRAM tests. Currently, the following test phases are performed:

- Voltage Cycling
- Mode Test
- Voltage Bounce
- March Up/Down
- Chip Heat
- Final Test

Voltage Cycling

During Voltage Cycling, the program cycles the test voltage while running various DDR2 memory tests. Some frequency drifts are normal for this test, as the module is periodically run at its lower voltage margin. The test can be skipped by pressing F1, or run again by pressing F2.

Mode Test

The new Mode Test explicitly checks various parameters of the DDR2 device. Currently it includes tests for the Burst Length, CAS Latency, Additive Latency and the Rtt/ODT controlled termination. (Please note that you must have firmware 2.30 or higher for this test).

Burst Length

DDR2 support Burst Lengths (BL) of 8 and 4. The Burst Length of 2 which is supported by SDRAM and DDR1 is not supported by DDR2 and future DDR generations.

CAS Latency

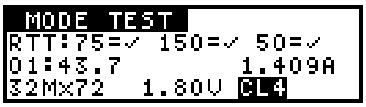
Please note that CAS Latency (CL) of 2 and 6 are optional, while all DDR2 devices must support CL of 3,4, and 5. The following screen shows a module that does not support CL2.

Additive Latency

DDR2 devices should support Additive Latency (AL) of 0, 1, 2, 3, and 4. The following screen shows the test result for AL3.

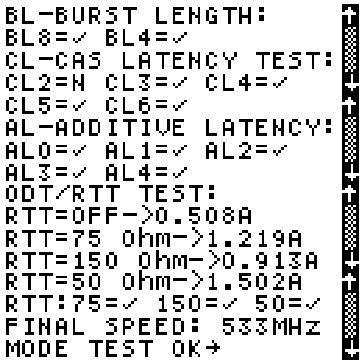
Rtt/ODT On-Die-Termination Test

The DDR2 devices employ a novel approach of built-in controlled termination, called On-Die-Termination (ODT). The ODT feature is controlled by a pair of input lines (ODT0 and ODT1), and special setup of the termination resistance Rtt. The Rtt setup supported by DDR2 technology is OFF, 75 Ohm, 150 Ohm and 50 Ohm. Please note that some devices do not support the 50 Ohm setup (they respond with 75 Ohm when the system is configured for 50 Ohm). We use our state-of-the-art current consumption/impedence determination circuitry to test the Rtt/ODT feature. The following screen shows the summary result for a module that supports all Rtt setup.

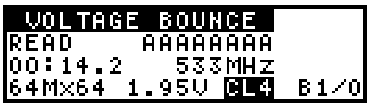


Detailed Mode results in the Test Log

Since the Mode Test includes a variety of sub-tests, many of which are very fast, the program Test Log is a very useful review tool. In the following four screens we capture a complete set of the Mode test results to demonstrate the extensive detail.

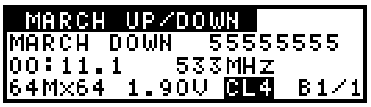


Voltage Bounce



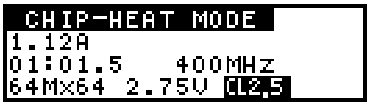
During Voltage Bounce, data is written to the module at a certain voltage (e.g. 1.95V) and then read at a different voltage (e.g. 1.75V). Some frequency drifts are normal for this test, as the module is periodically run at its lower voltage margin. The test can be skipped by pressing F1, or run again by pressing F2.

March Up/Down Test



During March Up/Down, the program attempts to catch cell interference errors. The test can be skipped by pressing F1, or run again by pressing F2.

Chip Heat Mode



During Chip-Heat Mode, we are using our proprietary technology to heat up the module, in preparation for the final phase of the Extensive Test. This mode can be skipped by pressing F1, or run again by pressing F2.

Final Test

The Final Test during Extensive Test is very similar to Basic Test. It incorporates the same two array tests. Typically, at this stage, the module has been heated up during Extensive Test and the Chip Heat Mode. This test can be repeated by pressing F2.

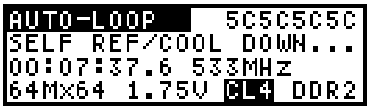
AUTO-LOOP TEST

The AUTO-LOOP test uses changing patterns to burn-in the module and to detect cell interferences. AUTO-LOOP continues until an error is detected or the user terminates the test by pressing the ESC key.

The AUTO-LOOP screen indicates the current loop number and the first

data of the current complex pattern. Note that each complex pattern includes an 8x72 bit array, so that the "AAAAAAAA" hex marker is just the first 32 bits of the first 64/72 bit extended word.

The screen also shows the voltage, the CL setup and current portion of the module that is being tested ("B1/1" means chip bank 1 of rank 1). Unless you have selected a specific CAS Latency (CL) value, the program automatically changes the CL setup every few loops. Similarly, unless you have setup a fixed voltage, the test voltages change every few loops. You can skip loops using F1, cycle the voltage using F2, or cycle the CL setup using F5.



During AUTO-LOOP, the program automatically cools down the tested module every 16 loops, so that the module's operation is checked with a changing temperature gradient. Other functions like self refresh or cke controlled power down mode are exercised during the cool down period.

4.8 RAMCHECK DDR2 S.O. DIMM CONVERTER

The RAMCHECK DDR2 S.O. DIMM Converter (p/n INN-8668-12-1) allows testing of 200-pin DDR2 S.O. DIMM modules on the DDR2 240-pin adapter (p/n INN-8668-12).

The converter is made in the shape of a standard 240-pin DIMM module. It has special electronics for RAMCHECK's auto-detection, and it is designed for low noise and short signal connections.

Operation

Place the converter on a flat surface that is covered with a proper anti-static sheet. Insert the 200-pin SO DIMM into socket J2, making sure that the module's pin-1 is facing left. Socket J2 is similar to the standard laptop sockets, and it has metal latch to insure proper retention of the module in place. We have selected the AMP gold plated sockets as the best available in the market. Once inserted, the module surface locks in parallel to the converter board, with the module's front side aligning with the converter's front side.

Insert the converter into the DDR2 adapter's 240-pin test socket as if it was a regular DDR2 module, making sure that pin-1 faces left. Press F1 to start the test, which generally follows the regular DDR2 test flow.

At the end of the test (RED power LED must be off), remove the converter and place it on the protected flat surface for removal of the tested S.O. DIMM module.

The converter is auto detected, and RAMCHECK's standby message should continue to prompt for a "DDR2 200p S.O. DIMM" until a regular 240-pin DDR2 module is tested.